AMENDMENT

Please replace the claims with the following:

1.   1. (Once Amended) An apparatus for compressing video data, comprising:

2.   a video input port, for receiving video data for a current video frame;

3.   a video input buffer coupled to the video input port, for storing video data

4.   from the video input port;

5.   a previous frame buffer, for storing at least a portion of a previous video

6.   frame;

7.   an operation unit coupled to the video input buffer and the previous frame

8.   buffer, for performing an operation between data from the video input buffer and

9.   data from the previous frame buffer; and

10.   a result buffer coupled to the operation unit, for storing the result of an

11.   operation from the operation unit;

12.   wherein the apparatus resides inside of a core logic chip for a computer

13.   system.

1.   2. (Unchanged) The apparatus of claim 1, including a memory port

2.   coupled to the previous frame buffer and the result buffer, for transferring data to

3.   and from a memory that stores video data from the video input port and result data

4.   from the result buffer.

1.   3. (Unchanged) The apparatus of claim 2, including a memory coupled to

2.   the memory port for storing the video data from the video input port and result

3.   data from the result buffer, wherein the video data is stored to in a current frame

4.   area in the memory and the result data is stored in a difference frame area in the

5.   memory.

1   4. (Unchanged) The apparatus of claim 3, wherein the memory stores a

2 current video frame and a previous video frame in the same location in the

3 memory, allowing the current video frame to be written over the previous video

4 frame.

1   5. (Unchanged) The apparatus of claim 3, wherein the memory also stores

2 instructions and data for a central processing unit of a computer system.

1   6. (Unchanged) The apparatus of claim 1, wherein the operation unit

2 performs an exclusive-OR operation between data from the video input buffer and

3 data from the previous frame buffer.

1   7. (Unchanged) The apparatus of claim 1, wherein:

2   the video input buffer stores a block of data from the video input port;

3   the previous frame buffer stores a block of data from the previous video

4 frame;

5   the result buffer stores a block of data from the operation unit; and

6   the operation unit performs an operation between a block of data from the,

7 video input port and a block of data from the previous frame buffer.

Please cancel claim 8 without prejudice

1   9. (Unchanged) The apparatus of claim 1, wherein the apparatus comprises

2 part of a video conferencing system.

1   10. (Unchanged) The apparatus of claim 1, including additional resources

2 within the apparatus, for compressing the video data from the video input port.

1   11. (Unchanged) The apparatus of claim 1, including a color space

2   conversion circuit coupled between the video input port and the video input

3   buffer.

1   12. (Unchanged) The apparatus of claim 1, wherein the video input buffer

2   is a register that stores less than one video frame.

1   13. (Once Amended) An apparatus for compressing video data,

2   comprising:

3   a video input port, for receiving video data for a current video frame;

4   a video input buffer coupled to the video input port, for storing video data

5   from the video input port;

6   a previous frame buffer, for storing at least a portion of a previous video

7   frame;

8   an exclusive-OR unit coupled to the video input buffer and the previous

9   frame buffer, for performing an exclusive-OR operation between data from the

10   video input buffer and data from the previous frame buffer;

11   a result buffer coupled to the operation unit, for storing the result of an

12   operation from the operation unit;

13   a memory port coupled to the previous frame buffer and the result buffer,

14   for transferring data to and from a memory that stores video data from the video

15   input port and result data from the result buffer; and

16   a memory coupled to the memory port for storing the video data from the

17   video input port and result data from the result buffer, wherein the video data is

18   stored to in a current frame in the memory and the result data is stored in a

19   difference frame in the memory;

4

A 2 cancel

20   wherein the apparatus resides inside of a core logic chip for a computer

21   system.

1   14. (Unchanged) The apparatus of claim 13, wherein the memory stores a

2 current video frame and a previous video frame in the same location, allowing the

3 current video frame to be written over the previous video frame.

1   15. (Unchanged) The apparatus of claim 13, wherein the memory stores

2 instructions and data for a central processing unit of a computer system.

1   16. (Unchanged) The apparatus of claim 13, wherein:

2   the video input buffer stores a block of data from the video input port;

3   the previous frame buffer stores a block of data from the previous video

4 frame;

5   the result buffer stores a block of data from the operation unit; and

6   the exclusive-OR unit performs an exclusive-OR operation between a

7 block of data from the video input port and a block of data from the previous

8 frame buffer.

Please cancel claim 17 without prejudice

1   18. (Unchanged) The apparatus of claim 13, wherein the apparatus

2 comprises part of a video conferencing system.

1   19. (Unchanged) The apparatus of claim 13, including a color space

2 conversion circuit coupled between the video input port and the video input

3 · buffer.

1   20. (Once Amended) A computer system including resources for

2   compressing video, comprising:

3   a central processing unit within the computer system;

4   a video input port, for receiving video data for a current video frame;

5   a video input buffer coupled to the video input port, for storing video data

6   from the video input port;

7   a previous frame buffer, for storing at least a portion of a previous video

8   frame;

9   an operation unit coupled to the video input buffer and the previous frame

10   buffer, for performing an operation between data from the video input buffer and

11   data from the previous frame buffer; and

12   a result buffer coupled to the operation unit, for storing the result of an

13   operation from the operation unit;

14   wherein the video input port, the video input buffer, the previous frame

15   buffer, the operation unit, and the result buffer reside inside of a core logic chip

16   for the computer system.